U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

B/O Form PTO 1390 **Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 U.S.C. §371**	*Attorney's Docket Number* TAMA.0003
	U S Application Number (if known) 10/070313

International Application Number	*International Filing Date*	*Priority Date Claimed*
PCT/JP99/06371	**16 November 1999**	**16 November 1999**

Title of Invention
DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM

Applicant(s) for DO/EO/US
Masayuki ITO and Yutaka YOSHIDA

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. §371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. §371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. §371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. §371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. A English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. §371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. §371(c)(5)).

Items 11 to 20 below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. §§1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. §§3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
14. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C, 1.821-1.825
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. Other items or information:

Application Number (if known)	International Application Number	Attorney's Docket Number
10/070313	PCT/JP99/06371	TAMA.0003

	CALCULATIONS	PTO USE ONLY
21. ☒ The following fees are submitted: **Basic National Fee** (37 C.F.R. §1.492(a)(1)-(5)): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO..... 1,040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO..... 890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. ..... 740.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... 710.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT	**$890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than □ 20 □ 30 months from the earliest claimed priority date (37 C.F.R. §1.492(e)).	**0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	14-20	0	x $18.00	**$0.00**	
Independent Claims	4 -3	1	x $84.00	**$84.00**	
Multiple Dependant Claims (if applicable)			+ 280.00	**$0.00**	
TOTAL OF ABOVE CALCULATIONS				**974.00**	
□ Entity claims small entity status. See 37 CFR1.27. The fees indicated above are reduced by 1/2.				**0.00**	
SUBTOTAL				**$ 974.00**	
Processing fee of **$130.00** for furnishing the English translation later than □ 20 □30 months from the earliest claimed priority date (37 C.F.R. §1.492(f)).				**$0.00**	
TOTAL NATIONAL FEE				**974.00**	
Fee for recording the enclosed assignment (37 C.F.R. § 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. §§ 3.28, 3.31). **$40.00** per property				**$40.00**	
TOTAL FEES ENCLOSED				**$ 1,014.00**	
				Amount to be Refunded:	**$**
				Charged:	**$**

a. ☒ A check in the amount of **$1,014.00** to cover the national fees and assignment recordation fee is enclosed.

b. ☒ Please charge my **Deposit Account Number 08-1480** in the amount of **$**_____ to cover the above fees if not covered by the enclosed check. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account Number 08-1480**. A duplicate copy of this sheet is enclosed.

d. □ Fees are to be charged to a credit card. **WARNING**: Information on this form may become public. Credit card information should not be included on this form. **Provide credit card information and authorization on PTO-2038.**

Note.: Where an appropriate time limit under *37 C.F.R. §1.94 or* §1.495 has not been met, a petition to revive *(37 C.F.R. §1.137(a) or (b))* must be filed and granted to restore the application to pending status.

Respectfully submitted,

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March 5, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)
	)
ITO et al	)
	)
Application Number: To Be Determined	)
	)
Filed: Concurrently Herewith	)
	)
FOR: DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM	)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicant has amended the claims in order to eliminate the multiple dependency of claims and thereby reduce the filing fee in accordance with standard U.S. practice. Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please substitute the claims currently on file with the following amended claims:

6. (Amended) The data processing system according to claim 4, wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

7. (Amended) The data processing system according to claim 4, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of data axquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meat by

the first information.

8. (Amended) The data processing system according to claim 4, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

Please add the following new claims:

12. The data processing system according to claim 5, wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

13. The data processing system according to claim 5, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of data axquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meat by the first information.

14. The data processing system according to claim 5, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

REMARKS

Applicant has amended claim 6 and added new claim 12, amended claim 7 and added new claim 13, and amended claim 8 and added new claim 14. No new matter has been added to the application as a result of this amendment.

In view of the above amendments and Applicant's comments stated herein, Applicant respectfully requests an early and favorable action on the merits.

Respectfully submitted,

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March 5, 2002

Marked Up Version of the Claims

6. The data processing system according to claim 4~~ or 5;~~ wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

7. The data processing system according to claim 4~~ or 5~~, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of data axquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meat by the first information.

8. The data processing system according to claim 4~~ or 5;~~ wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

Application for
UNITED STATES LETTERS PATENT

Of

MASAYUKI ITO

and

YUTAKA YOSHIDA

DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM

SPECIFICATION

TITLE OF THE INVENTION

DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to a data processing device such as a microprocessor or DSP (Digital Signal Processor) having a cache memory and further relates to a data processing system having a burstable memory along with such a data processing device.

In a data processing system using a data processing device such as a microprocessor, a memory preferably for use in attaining high-speed data access or high data transfer performance is a memory that supports burst operations (they are also called burst transfers), typified by a synchronous DRAM (Dynamic Random Access Memory). More specifically, according to this type of memory, an operation control system including circuits such as an internal address counter inside the memory allows reading and writing continuous data at high speed, thereby facilitating the realization of a high-speed, high-performance processing system.

The synchronous DRAM has a mode register. The mode register designates the operation mode thereof. Mode

information including burst length information, which is also called a burst transfer length or block transfer length for the synchronous DRAM, is set in the mode register according to a setting program such as a system initialization program executed after power on reset of a processing system. To set information such as the burst length information, a set period different from the burst operations is required. That is, it relatively takes time to set the mode information in the mode register. On this account, the burst length information once set in accordance with power on reset is not changed later in general.

Here, in the burst operations, when the burst length is set greater, an amount of data that can be transferred by access at one time to the synchronous DRAM becomes large, and thus the high data transfer performance can be obtained in the case of transferring a mass amount of data. However, when an amount of data smaller than the set burst length is transferred, unnecessary data transfer cycles are increased and the data transfer performance is deteriorated because block transfers are conducted according to the set burst length.

In the memory that supports burst transfers, typified by the synchronous DRAM, in burst transfers a wraparound function is supported in which transfer can be started from data at an arbitrary address between the boundaries of burst transfers. As for location addresses between the boundaries,

the first location of data to be accessed is designated from outside, and the subsequent location addresses are created by an internal counter such as a column address counter inside the memory. The SDRAM is considered to have an access unit of four bytes and a burst length of 16 bytes, for example, in which a column address in a byte unit is preset in the column address counter, and it sequentially undergoes counter operations for three times from the least significant bit to the fourth bit, starting from the preset address, whereby continuous access operations are performed. For example, when data locations in a four-byte unit between the boundaries of burst operations are set to an address of N + 00 (hereafter, it is denoted as @00), @04, @08 and @12, data access is performed by wraparound in order of @08, @12, @00, and @04, where the first location of data accessed in burst operations is set to @08.

Utilizing the wraparound function can acquire data required by a CPU from an external memory at the start of burst transfers. Accordingly, in a cache mishit, for example, the number of cycles that the CPU waits for data can be reduced.

The memory that supports burst access, typified by the synchronous DRAM, gives the characteristics according to the burst length as described above. Thus, desirably, the type of memory can be adapted to both demands of setting the burst length greater and setting it smaller. Then, the inventors

investigated the effectiveness of a control method of utilizing both of memories performing wraparound at a different burst length, such as a synchronous DRAM having a burst length of 32 bytes and a synchronous DRAM having a burst length of 16 bytes.

The inventors revealed the following items according to the investigation. More specifically, the order of data returned from the synchronous DRAM in the wraparound operation is varied in the case where the synchronous DRAM having a burst length of 16 bytes undergoes burst operations by wraparound starting from the eighth byte in the column address location of 16 bytes and in the case where the synchronous DRAM having a burst length of 32 bytes undergoes burst operations by wraparound starting from the eighth byte in the column address location of 32 bytes. Thus, the need occurs in which a memory control circuit for controlling the synchronous DRAM is configured to have a scheme of recognizing or eliminating a mismatch of data arrangement due to the burst length difference.

The two following techniques can be named as the scheme to do so, for example.

A first technique is that two sets of data of 16 bytes returned from the memory having a block transfer length of 16 bytes are conformed to the same data order as the data order in the wraparound operation of a burst length of 32 bytes. In

this case, a buffer memory and an aligner for sorting data are set along with the memory control circuit. The memory control circuit performs the control operation in which in burst read operations, for example, the memory control circuit temporarily buffers data outputted from the memory in the buffer memory, and then it uses the aligner to sort data for data output so that two sets of data having undergone wraparound in 16 bytes are conformed to the data order obtained by the wraparound operation of 32 bytes. In the case of the first technique, extra waiting time is needed in data buffering for sorting data.

A second technique is that a mismatch of the order of returning data is prevented from occurring by establishing a restriction where a start memory access address has the boundary fixing of 16 bytes. Accordingly, the data order when burst operations are performed twice in a burst length of 16 bytes is conformed to the data order when a burst operation is performed once in a burst length of 32 bytes.

However, the inventors took notice that the both techniques described above are accompanied by the deteriorated data processing performance. Hereafter, it will be described.

Here, the microprocessor is considered to have a CPU, a cache memory and a memory control circuit for having access to external memories including an external synchronous DRAM. Now, consider the case where a cache line length of the cache

memory is 32 bytes, a cache mishit is made when the CPU starts access at an address of N + 08 (N is a multiple of 32) in a memory, the external memories are accessed according to that, cache lines are filled, and then the CPU continuously requests data at sequential addresses of N + 12, N + 16, N + 20, N + 24, and N + 28. Additionally, the access to such a sequential addresses can be considered to be a natural example frequently generated in the case of instruction access or in processing data arranged in continuous areas. Hereafter, data at an address of N + 08 is denoted by @08, and data at an address of N + 12 is denoted by @12.

Under the conditions, in the first technique, the data order obtained from the memory according to the burst operations of a block transfer length of 16 bytes is considered to be in order of @08, @12, @00, @04, @24, @28, @16, and @20, for example. In sorting it into a data order as similar to the data order in the case of the burst operations of a burst length of 32 bytes and returning it to the cache memory, some penalty cycles are generated, which cause the bus performance or data processing performance of the CPU to be deteriorated. More specifically, in the case of that data order, the data order corresponding to the burst operations of 32 bytes is in order of @08, @12, @16, @20, @24, @28, @00, and @04. In sorting the data in that order and retuning it to the cache memory, data @16 needed to return to third position corresponding to

the burst operations of 32 bytes arrives from the memory in the seventh place in the burst operations of 16 bytes, which will generate at least four penalty cycles.

In the second technique, both the data order from the external memories and the data order to the cache corresponding to the case where the CPU first needs data @08 are in order of @00, @04, @08, @12, @16, @20, @24, and @28. That is, data @08 required first by the CPU is to be the third data. In response to this, the CPU will wait the arrival of the first data needed by the CPU for at least two cycles. In this manner, the deteriorated performance of the CPU occurs in the second technique as well.

Additionally, the ninth page and Table 2 of MICROPROCESSOR REPORT VOL. 10, NO. 2, FEBRUARY 12, 1996 describe that the order of the cache fill is controlled so as to put a missed word of the cache memory first in a 32-byte microprocessor. However, it does not take notice of the relationship between the burst length of the synchronous DRAM and the data order of cache fill.

A purpose of the invention is to provide a data processing device capable of shortening waiting time of a CPU until acquiring data associated with cache miss and of contributing to the enhanced data processing performance, even using a memory burstable in a size shorter than a cache line length of a cache memory and having a wraparound function, and to

further provide a data processing system.

Another purpose of the invention is to provide a data processing device having fewer penalty cycles in memory access and capable of enhancing the bus performance and the CPU performance, even connecting and utilizing a plurality of memories having a wraparound function and a different burst length, and to further provide a data processing system.

Still another purpose of the invention is to provide a data processing device capable of responding to various connection configurations and utilization forms of burstable memories having a wraparound function.

The above and other purposes and the novel features of the invention will be apparent from the following description of the specification and accompanying drawings.

SUMMARY OF THE INVENTION

[1] The data processing device has a CPU, a cache memory accessible by the CPU, a cache control part for controlling the cache memory, and a memory control part accessible to memories in response to a cache mishit of the cache memory. When the memory control part has access to a burstable memory in response to a cache mishit, it forms first information for indicating a burst length of the memory to a cache line length of the cache memory, and it can control a single or plurality of burst operations necessary to obtain a data length meeting

the cache line length according to the first information. The cache control part can control the cache fill operation of filing data acquired in the single or plurality of burst operations in the cache memory by wraparound according to the first information.

According to the scheme described above, the first information reveals the burst length of the memory to be accessed to the cache line length, the number of burst operations corresponding to the memory to be accessed is controlled according to this, and block data corresponding to the cache line length can be acquired from the memory in the burst operations. The cache control part allows the block data, which is being transferred to the cache memory in the wraparound operation, to be filled in the cache, as meeting the acquired block data to the burst length learned from the first information. On this account, data outputted from the memory does not need to be sorted by an aligner. Additionally, the restriction where the top boundary of the data block to be the object for burst operations is fixed to a start access address does not need to be provided. Thus, the data processing device can shorten waiting time of the CPU until acquiring data in a cache miss, even using the memory burstable in a size shorter than the cache line length of the cache memory and having a wraparound function, and therefore it can contribute to the enhanced data processing performance.

In the cache fill operation, the cache control part can be configured to receives the inputs of address information in a cache mishit, the first information and a synchronization signal synchronous with a delimiter of data obtained in the burst operations by the memory control part, to perform the wraparound control starting from the address information in the range of the burst length meant by the first information, and to create cache fill addresses for determining the data order of cache fill in synchronism with the synchronization signal.

Accordingly, the cache fill operation can proceed as following the operation where the memory control part sequentially reads data out of the memory in burst operations in response to a cache mishit. Regardless of a burst length of the memory, the high-speed cache fill operation can be assured.

The memory control part can be configured to control burst operations in which in having access to a memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a burst operation by wraparound starting from a data location at an address in the cache mishit in the first burst operation, and it controls burst operations starting from the top boundary of the data block defined by the burst length in the subsequent burst operations.

In view of the fact that a program or certain data is

often located at sequential addresses, as for access other than the first access among a plurality of access in burst operations, when the memory is accessed from the top boundary defined by burst length, data to be accessed first by the CPU is to reach the cache memory or CPU first in sequential data access, as described above. Therefore, it is useful to enhance the data processing performance.

According to the data processing device described above, when a burst length (16 bytes, for example) relatively shorter than the cache line length (32 bytes, for example) of the cache memory is set in the memory, a plurality of data blocks outputted by wraparound from the memory performing burst access operations can be joined and filled in the cache memory. Furthermore, in the case where write through is adopted as one process for a cache write hit of the cache memory, when write data is written into the memory from a write through buffer shorter than the cache line length (eight byte, for example), there are fewer unnecessary data transfer cycles because of the relatively shorter burst length. As for eight bytes in the latter half of the burst access operation at this time, the actual data write operation can be suppressed by data masking.

Accordingly, the data processing device can suppress unnecessary cycles to the minimum in transferring relatively small data of eight bytes without deteriorating the performance

of efficiently transferring high-capacity data of 32 bytes to the cache memory, and thus it can enhance the data processing performance.

[2] The data processing system has a data processing device having a CPU and a cache memory, and a memory connected to the data processing device, the memory is burstable and configures a main memory for the cache memory. The memory may be single or plural. The burst length of each memory may be different or the same. The cache memory has a cache line length of L bytes. The memory is burstable by wraparound in the range of a burst length in bytes, where L times one over two to the n-th power (n is a natural number). At this time, the data processing device performs control in which it forms first information for indicating the burst length of the memory to the cache line length of the cache memory in response to a cache mishit of the cache memory, it allows the memory into burst operations for a single or plurality of times necessary to obtain a data length meeting the cache line length according to the first information, it joins a plurality of block transfer data thereby acquired, and it returns data of L bytes to the cache memory.

According to the data processing system, when a burst length (16 bytes, for example) relatively shorter than the cache line length (32 bytes, for example) of the cache memory is set in a first memory, a plurality of block data outputted

from the burstable memory by wraparound can be joined and filled in the cache memory. When the data processing system includes a second memory set up with the same burst length as the cache line length, it allows the cache fill operation responding to the burst length of the second memory in processing a cache mishit for the second memory.

Additionally, in the case where write through is adopted as a process for a cache write hit of the cache memory, when write data is written into the first memory from a write through buffer shorter than the cache line length (eight bytes, for example), there are fewer unnecessary data transfer cycles because of the relatively shorter burst length. As for eight bytes in the latter half of the burst access operation at this time, the actual data write operation can be suppressed by data masking. When the second memory set up with the same burst length as the cache line length is the object to be written by write through, unnecessary cycles are increased as compared with the first memory, even performing write mask. Even so, in a state that the second memory is temporarily removed from the object for cache, it is possible to increase an amount of data accessible or transferred at one time.

Accordingly, the data processing system can suppress unnecessary cycles as much as possible in transferring relatively small data of eight bytes without deteriorating the performance of efficiently transferring high-capacity data of

32 bytes to the cache memory, it can realize various connection configurations or utilization forms of a plurality of memories having a different burst length, and thus the data processing performance can be enhanced in the data processing system.

Also in the data processing system, the data processing device can be configured to perform control of filling data, which is being transferred in the wraparound operation, in the cache memory according to the first information, the data has been acquired in the single or plurality of burst operations. Also at this time, in the cache fill operation, the data processing device can be configured in which it creates a synchronization signal synchronous with a delimiter of data obtained from the memory in the burst operations, it controls wraparound starting from the address information in the range of a burst length meant by the first information, and it creates cache fill addresses for determining the data order of cache fill in synchronism with the synchronization signal. Furthermore, the data processing device can be configured in which in having access to a memory in burst operations for a plurality of times in response to a cache mishit, it controls a burst operation by wraparound starting from the data location at the address in the cache mishit in the first burst operation, and it controls burst operations starting from the top boundary of the data block defined by the burst length in the subsequent burst operations.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

Fig. 1 depicts a block diagram illustrating one example of a data processing system in the invention;

Fig. 2 depicts a block diagram illustrating one example of a detailed block transfer length determining part;

Fig. 3 depicts a block diagram illustrating one example of an external memory address generating circuit;

Fig. 4 depicts an illustration exemplifying the address generation rule of the generation logic for subsequent access addresses;

Fig. 5 depicts a timing chart exemplifying burst operations for a synchronous DRAM set up with a burst length of 32 bytes;

Fig. 6 depicts a timing chart exemplifying burst operations for a synchronous DRAM set up with a burst length of 16 bytes;

Fig. 7 depicts a block diagram illustrating one example of the logic configuration for generating a cache access address and a memory access address in a cache control part;

Fig. 8 depicts an illustration exemplifying the address generation logic of a cache fill address generating circuit;

Fig. 9 depicts a timing chart illustrating the cache fill operation by a microprocessor shown in Fig. 1, also including comparative examples; and

Fig. 10 depicts a block diagram illustrating another example of the data processing system in the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 depicts one example of the data processing system in the invention. The data processing system depicted in the same drawing is typically provided with a microprocessor 1, which is one example of the data processing device in the invention, a synchronous DRAM 2, which is one example of a burstable external memory, and a ROM (Read Only Memory) 14. It may be provided with other peripheral circuits other than the synchronous DRAM 2 and the ROM 14.

Although the microprocessor 1 is not defined particularly, it has a CPU 3, a cache memory 4, a cache control part 5, and a memory control part 6. They are formed on one semiconductor substrate (semiconductor chip), for example. Although data buses 8, 9 and 10 are not defined particularly, they are considered to be four bytes (32 bits).

The CPU 3 has a control part and an execution part, not shown in the drawing. The execution part has a general purpose register file and a computing unit, for example. The control part decodes fetched commands and it controls the operation

of the execution part.

The cache memory 4 has a so-called data array. The data array is configured of an SRAM (Static Random Access Memory), for example, and it has a matrix of memory cells. A selection terminal of the memory cells is connected to a word line at every row, for example, and a data input/output terminal of the memory cells is connected to a complementary bit line at every column. In the data array, the word line is selected by an index address given from the cache control part 5. A unit at every row selected by the index address is a cache line in the data array. Although the cache line is not defined particularly, it has a cache line length of 32 bytes. For the selected cache line, a long word selection signal given from the cache control part 5 performs the selection of four bytes. The index address and the long word selection signal are denoted by a cache access address signal 7 in the drawing.

The cache control part 5 has a so-called address array and a cache control logic. The address array is also configured of the SRAM as similar to the data array. The address array has tag fields for each of the cache lines one on one. The tag field holds valid bits for indicating the effectiveness of the corresponding cache line tag or the cache line. The tag field is also selected by the index address. The cache control logic determines whether a cache hit or cache mishit, and it controls cache fill when a cache mishit.

The memory control part 6 performs bus control for having access to the synchronous DRAM 2 or ROM 14 according to the instruction of the CPU 3 or cache control part 5. The memory control part 6 is connected to the synchronous DRAM 2, typically shown, through the external bus 10 and an external address bus 13. Control buses for transmitting control signals such as a strobe signal for access to the external busses or external memories are omitted from the drawing. The memory control part 6 can be understood as a so-called bus state controller, or a part of a memory controller contained therein.

A part of an effective address 11 outputted by the CPU 3 is set to be the index address. The cache control logic compares the tag of the tag field indexed in the address array with a tag address contained in a part of the effective address 11. It is considered to be a cache hit when they match each other, whereas it is considered to be a cache mishit when they do not match each other.

In the read access by the CPU 3, when it is a cache hit (cache read hit), data of four bytes corresponding to the indexed cache line is fed to the CPU 3 through the data bus 8. When it is a cache mishit (cache read mishit) in the read access, the cache control part 5 generates a memory access address 12 and it gives a memory access request MREQ to the memory control part 6 along with the memory access address 12. Accordingly, the memory control part 6 reads data of one cache

line from the synchronous DRAM 2, for example, and it feeds the read data to the cache memory 4 through the data bus 9. In synchronism with this, the cache control part 5 generates the cache access address 7 and it fills the data in a required cache line. Additionally, the cache control part 5 stores a tag corresponding to the data of the cache line in a tag field corresponding to the cache line. At this time, data in a cache miss is given to the CPU 3 through the data bus 8.

In the write access by the CPU 3, when it is a cache hit (cache write hit), the CPU 3 feeds write data to four bytes of the corresponding cache line indexed through the data bus 8. When it is a cache mishit (cache write mishit) in the write access, the cache control part 5 generates the memory access address 12 and it gives the memory access request MREQ to the memory control part 6. The memory control part 6 reads data of one cache line from the synchronous DRAM 2, for example, according to the memory access address 12, and it gives the read data to the cache memory 4 through the data bus 9. In synchronism with this, the cache control part 5 fills the data in a cache line, and it stores a tag corresponding to data of the cache line in the tag field corresponding to the cache line.

As for a scheme of maintaining the match between data held by the cache memory 4 and data stored in the external memory such as the synchronous DRAM 2, a method of write through is adopted, for example. That is, the cache memory 4 has a write

through buffer for holding write data when a cache write hit, not shown in the drawing. When a cache write hit, the cache control part 5 writes write data in the cache write hit into the cache memory 4, and then it gives an instruction of writing into the corresponding address of the corresponding synchronous DRAM 2 to the memory control part 6. Accordingly, the memory control part 6 controls writing data held in the write through buffer into the synchronous DRAM 2.

The synchronous DRAM 2 has a memory cell array having a matrix of dynamic memory cells in which the information storage format is performed dynamically through a storage capacitor as similar to a DRAM, and the refreshment of storage information is also needed. A huge difference from the DRAM is in that the synchronous DRAM 2 is operated synchronously with an external clock signal and it is burstable by wraparound. For example, it has a column address counter for latching a column address signal fed from outside in which it sequentially updates column addresses by the column address counter and it can efficiently perform the continuous data access operation, starting from a preset value of the column address counter as maintaining the word line selecting state by row addresses. The number of continuous data access is called a burst length, and the column address counter undergoes counter operations only for the number of times defined by the burst address. For instance, in a synchronous DRAM having an access unit of four

bytes and a burst length of 16 bytes, the continuous access operation can be performed in which the column address in a byte unit is preset in the column address counter and the column address counter undergoes counter operations for three times from the least significant bit to the fourth bit, starting from the preset address. Therefore, when the base point of access in a four-byte unit is not at the boundary of the location in the column data location of 16 bytes, the counter address by the column address counter is returned to the boundary of the previous column data location of 16 bytes from the subsequent column data location of 16 bytes in the midway for address counting. That is, the access order of the burst operations is performed by wraparound within the column data location of 16 bytes.

The burst length is set in a mode register of the synchronous DRAM 2. For example, a part of memory control data 15 set in the memory control part 6 from the CPU 3 in the power on reset processing is also initialized in the mode register by the CPU 3 as data for indicating a burst length. Although a burst length is not defined particularly, it can be set selecting from 16 or 32 bytes. The operation of the synchronous DRAM 2 is instructed according to the states of signals such as row address strobe (RAS), column address strobe (CAS), write enable (WE), data mask (DM), and data strobe (DQS). The memory control part 6 generates the signals. Commands are defined according

to each of the specific states of the signals, and the synchronous DRAM 2 performs operations according to the instruction of the command. For example, an active command accompanied by the row address signal instructs a word line selection operation. A read command accompanied by the column address signal instructs a read operation for the memory cells of the word line already activated. Additionally, a write command accompanied by the column address signal instructs a write operation for the memory cells of the word line already activated. The read operation and the write operation are performed in wraparound-capable burst access in a burst length set in the mode register. In the write operation, in an access cycle where the data masking (DM) signal is set enable, only the access cycle is consumed and the actual data write is suppressed.

Next, the memory control and the cache fill operation corresponding to the burst length of the synchronous DRAM 2 will be described.

First, the summary thereof will be described in accordance with Fig. 1. A block transfer length determining part 20 and an external memory address generating part 30 are typically depicted in the memory control part 6. The block transfer length determining part 20 forms wraparound information WRPA that is the first information for indicating the burst length of the synchronous DRAM 2 to the cache line

length (32 bytes) of the cache memory 4 in having access to the synchronous DRAM 2 in response to the memory access request MREQ from the cache control part 5 due to a cache mishit. The external memory address generating part 30 controls a single or plurality of burst operations necessary to obtain the data length meeting the cache line length and it burst-reads data out of the synchronous DRAM 2, according to the wraparound information WRPA. It may activate burst access twice when the burst length is 16 bytes, whereas it may activate burst access once when the burst length is 32 bytes. The top of burst read is data of an address in a cache miss. The cache control part 5 generates cache fill addresses for writing data of 32 bytes read by the memory control part 6 in burst read into the cache memory 4 by wraparound at every four bytes. The data block of one wraparound operation at this time is matched with the burst length of the synchronous DRAM 2. It undergoes wraparound operations at every range of a 16-byte address when the burst length is 16 bytes, whereas it undergoes wraparound operations at every range of a 32-byte address when the burst length is 32 bytes. The cache fill address in the wraparound operations is the index address and the long word selection signal 7. The long word selection signal is synchronous with a data ready signal DRDY for indicating a delimiter of data that the memory control part 6 reads in burst read and outputs to the data bus 9 at every four bytes.

Fig. 2 depicts a detailed example of the block transfer length determining part 20. The block transfer length determining part 20 has an access request determining circuit 22, memory control registers 23, and a block transfer length determining circuit 24. In the memory control registers 23, the CPU 3 initializes a data bus width for an external address area of the microprocessor 1, the number of access cycles, external memory information 15 such as a burst length. Burst length data for indicating a burst length having been set in the synchronous DRAM 2 by the CPU 3 is also set in the memory control registers 23.

The access request determining circuit 22 receives the inputs of the memory access request MREQ and the memory access address 12 from the cache control part 5, and it activates a detection signal 25 when an object to be accessed is the synchronous DRAM 2. Furthermore, the access request determining circuit 22 detects a memory access request by the memory access request MREQ, it decodes the memory access address 12, it selects an area according to the area to be accessed, and then it generates an access area selection signal (not shown). This access area selection signal is utilized as a chip selection signal or memory enable signal for memories, for example.

The block transfer length determining circuit 24 receives the inputs of the detection signal 25 and information

26 for a burst length of the synchronous DRAM 2 set in the memory control registers 23 and it outputs the wraparound information WRPA. Here, the burst length of the synchronous DRAM 2 is 16 or 32 bytes and the cache line length of the cache memory 4 is 32 bytes. Thus, although the wraparound information WRPA is not defined particularly, it is information of one bit; the logical value "0" means a burst length of 16 bytes, and the logical value "1" means a burst length of 32 bytes, for example.

Fig. 3 depicts one example of the external memory address generating part 30. The external memory address generating part 30 has an address buffer 31, a subsequent access address generating circuit 32, and a selector 33. The external memory address generating part 30 receives the memory access address 12 from the cache control part 5 and then it keeps the memory access address 12 in the address buffer 31. Subsequently, it allows the selector 33 to select the address kept in the address buffer 31 and to output the address to the address bus 13 as an external memory address 16. When the area selection by the request determining circuit 22 at this time is the synchronous DRAM 2, the synchronous DRAM 2 is selected as a chip, and a read or write command is fed through a synchronous DRAM control logic inside the memory control part 6, not shown. Thus, the synchronous DRAM 2 is allowed into burst operations. When the wraparound information WRPA is the logical value "1", the burst operation is finished for one time. When the wraparound

information WRPA is the logical value "0", the subsequent access address generating circuit 32 performs +16 to an address (byte address) of the address buffer 31, for example, according to the after-mentioned address generation logic and it generates the first address in the next burst operation, in order to allow the synchronous DRAM 2 into burst operations twice. The details of the generation logic for the subsequent access addresses will be described later. In the second-time burst operation, the selector 33 selects the output of the subsequent access address generating circuit 32 to feed it to the synchronous DRAM 2.

Fig. 4 exemplifies the rule of the generation logic for the subsequent access addresses. Here, supposing that the cache line length is 32 bytes, the burst length of the synchronous DRAM is 32 or 16 bytes, and the data bus width is four bytes, where N is a multiple of 32, data of four byte from an address of N is denoted by D1, and data of four byte from an address of N + 4 is denoted by D2.

In Fig. 4, a first access address means a start address of the first-time burst operation, and a second access address means a start address of the second-time burst operation necessary when the burst length is 16 bytes. The access address at the second time is not set to a value where the access address at the first time is uniformly added with 16 bytes. In the case where the burst length is 16 bytes, the access address

at the second time is set to an address of N + 16 when the first access address is addresses of N + 4, N + 8, and N + 12. Therefore, the data output is in order of addresses at the second-time burst access. In view of the fact that a program or certain data is often located at sequential addresses, as described above, as for access except the first access among a plurality of access in burst operations, when the memory is accessed from the top of the boundary defined by the burst length, data to be accessed first by the CPU 3 arrives at the cache memory 4 or CPU 3 first in the continuous data access, and thus it is useful to enhance the data processing performance. In conformity to this, the second-time access address is set to an address of N + 0 when the first access address is also addresses of N + 20, N + 24, and N + 28.

Fig. 5 exemplifies a timing chart of the burst operations for the synchronous DRAM 2 set up with a burst length of 32 bytes. Here, a start transfer address given by the external memory address generating part 30 is an address of N + 8, and the wraparound information means 32 bytes. In this case, the synchronous DRAM does of course not need the second-time burst access. In Fig. 5, it should be understood that a bank active command, not shown in the drawing, has been issued prior to the read command and the word selection operation has already been completed. As apparent from Fig. 5, a burst read of 32 bytes is performed by wraparound in order of D3, D4, D5, D6,

D7, D8, D1, and D2.

Fig. 6 exemplifies a timing chart of the burst operations for the synchronous DRAM 2 set up with a burst length of 16 bytes. Here, it should be under stood that the first start transfer address given by the external memory address generating part 30 is an address of N + 8, the start transfer address for the burst operation at the second-time is also set to an address of N + 16 in accordance with Fig. 4, the bank active command, not shown in the drawing, has first been issued prior to the read command, and the word selection operation has already been completed. As apparent from the logic shown in Fig. 4, a burst read is performed by wraparound in order of D3, D4, D1, and D2 in the first-time burst operation. A burst read is performed in order of D5, D6, D7, and D8 from the top of the data block in the second-time burst operation.

Fig. 7 depicts one example of the logic configuration for generating cache access addresses and memory access addresses in the cache control part 5. The cache control part 5 has an address buffer 40, a memory access address generating circuit 41, a cache fill address generating circuit 42, and a selector 43. The cache control part 5 receives an effective address 11 from the CPU 3 and it keeps the effective address 11 in the address buffer 40. Then, it allows the selector 43 to select the address kept in the address buffer 30 and to feed the address to the cache memory 4 as the cache access address

7. When a cache entry of the cache line corresponding to the cache access address is a cache mishit, the memory access address generating circuit 41 generates the memory access address 12 in the cache mishit in response to this. The access control of the synchronous DRAM 2 by the memory control part 6 using the memory access address 12 is as described above.

The cache fill address generating circuit 42 generates the cache fill addresses for writing data of 32 bytes that the memory control part 6 has read from the synchronous DRAM 2 in burst read into the cache memory 4 by wraparound at every four bytes. The cache fill address generating circuit 42 at this time receives the input of the wraparound information WRPA so as to allow the data block in wraparound operations to meet the burst length of the synchronous DRAM 2, and it allows wraparound operations in the range of every address of 16 bytes when the burst length is 16 bytes, whereas it allows wraparound operations in the range of every address of 32 bytes when the burst length is 32 bytes. The first address of the cache fill addresses in wraparound operations is an address in a cache miss held in the address buffer 40. The cache fill addresses in wraparound operations are the index address and the long word selection signal 7 as described above. When the memory control part 6 outputs data having been read out of the synchronous DRAM 2 in burst read to the data bus 9 at every four bytes, it outputs a data ready signal DRDY for indicating

the delimiter of the data. The cache fill address generating circuit 42 sequentially increments the first address of the cache fill addresses by +4 in synchronism with the data ready signal DRDY.

Fig. 8 exemplifies the address generation logic of the cache fill address generating circuit 42. The first address of the cache fill addresses is determined by the effective address in a cache mishit. Thus, the cache fill addresses of a burst length of 32 bytes and 16 bytes and dada corresponding thereto are shown at every effective address in a cache mishit in pairs in Fig 8.

In Fig. 8, N is set to a multiple of 32, data at an address of N is called D1, data at an address of N + 4 is D2, and data at an address of N + 28 is D8. At this time, when the effective address from the CPU 3 is an address of N + 8 and the wraparound information means 16 bytes, the data order returned from the synchronous DRAM 2 is in order of D3, D4, D1, D2, D5, D6, D7, and D8. To fill them in the proper locations of cache, the cache fill address generating circuit 42 generates the cache access address 7 so as to sort the cache fill addresses in order of N + 8, N + 12, N, N + 4, N + 16, N + 20, N + 24, and N + 28, in accordance with the data ready signal DRDY issued by the memory control part 6 in synchronism with data change.

Fig. 9 depicts the above-described cache fill operation by the microprocessor 1, also including comparative examples.

In the related art, when an address in a cache mishit is set to an address of N + 8, data read out of a synchronous DRAM of a burst length of 32 bytes in burst operations is in order of @08, @12, @16, @20, @24, @28, @00, and @04, as shown in (A) in Fig. 9. Data read out of a synchronous DRAM of a burst length of 16 bytes in twice burst operations is in order of @08, @12, @00, @04, @24, @28, @16, and @20, as shown in (B) in Fig. 9. In this manner, the data order read out of the synchronous DRAM is varied from a burst length. In the related art in which a data aligner for conforming the data order to the data order in burst operations of 32 bytes is provided before cache fill so as not to perform cache fill with this mismatch, four penalty cycles in data sorting are generated, as shown in (C) in Fig. 9, and thus the bus performance is deteriorated. On the other hand, in the related art in which the start access address has the restriction of boundary fixing, as shown in (D) in Fig. 9, since the first data is fixed to an address of N + 0 for boundary fixing in spite of having been generated a cache mishit at an address of N + 8, data to be required first by the CPU 3 cannot be fed in the first place to generate two cycles of penalty, thereby causing the CPU performance to be deteriorated. However, in the microprocessor 1, the process of buffering and sorting burst read data is not performed, and the memory control part generates cache fill addresses corresponding to the burst length of burst read data according to the wraparound

information, as shown (E) in Fig. 9. Therefore, the penalty is not generated as shown in (C) in Fig. 9. Additionally, as apparent from (E) shown in Fig. 9, the start address of the burst access does not have the restriction of boundary fixing, and thus the penalty is also not generated as shown in (D) in Fig. 9. Furthermore, the first address of the second-time burst access is set to the top of the boundary according to the logic shown in Fig. 4, as (E) shown in Fig. 9. Therefore, when the CPU 3 requires continuous data, the request can be responded promptly.

The operation will be described more specifically, with reference to Fig. 9. In the case where the CPU 3 starts access from an address of N + 08, memory access due to a cache miss is generated and the CPU 3 continuously requires data of sequential addresses of N + 12, N + 16, N + 20, N + 24, and N + 28, the data order from the synchronous DRAM is in order of @08, @12, @00, @04, @24, @28, @16, and @20 in the scheme of (C) shown in Fig. 9. Data @16 that the CPU 3 requires third arrives in the seventh place from the memory, and thus at least four penalty cycles are generated. However, when using the scheme of (E) shown in Fig. 9, the data order from the synchronous DRAM 2 is in order of @08, @12, @00, @04, @16, @20, @24, and @28. Data @16 that the CPU 3 requires third is allowed to arrive in the fifth place from the synchronous DRAM 2, and the penalty cycle can be reduced to two cycles. Thus, the

enhanced data processing performance by the CPU 3 can be realized. Such the access to the sequential addresses is generated with great frequency in the case of instruction access or continuous data processing. Therefore, the great effect can be obtained in enhancing the data processing efficiency.

Moreover, the cache control part 5 receives the wraparound information WRPA along with data from the synchronous DRAM 2, whereby access can also be started from the location other than the boundary top of the data block defined by burst length and the data processing performance by the CPU can be enhanced. More specifically, in (D) shown in Fig. 9, data required first by the CPU is data @08, but the data order returned from the memory has the restriction of starting from the top of the memory block. Thus, memory access from data @08 cannot be performed, the start burst transfer address is turned to be an address of N + 0, and the data order retuned from the memory is in order of @00, @04, @08, @12, @16, @20, @24, and @28. Consequently, data @08 is in the third place, and the CPU has to wait the arrival of the first data for two cycles, thereby causing the deteriorated data processing performance of the CPU. However, when using the control scheme typified by (E) shown in Fig. 9, the start burst transfer address can be turned to be an address of N + 8, the data order from the memory is in order of @08, @12, @00, @04, @16, @20,

@24, and @28. Data @08 required first by the CPU 3 is allowed to arrive in the first place from the synchronous DRAM 2, the penalty cycles of the CPU 3 can be reduced to two cycles, and therefore the enhanced data processing performance of the CPU 3 can be realized.

Besides, the process of (E) shown in Fig. 9 adapts the generation logic for the cache fill addresses shown in Fig. 8. Thus, as shown the same drawing, when data @010 required third by the CPU 3 is obtained, four penalty cycles generated in (C) shown in Fig. 9 can be suppressed to two cycles. Also in this point, the data processing performance by the CPU 3 can be enhanced.

The operation and effects obtained by the above-described microprocessor 1 will be organized and described.

In the microprocessor 1, the memory control part 6 learns the burst length of the memory to be accessed (synchronous DRAM 2) to the cache line length according to the wraparound information WRPA, it controls the number of burst operations corresponding to the memory 2 to be accessed according to this, and it can obtain the block data corresponding to the cache line length from the synchronous DRAM 2 in burst operations. The cache control part 5 allows the acquired block data to be filled in the cache memory 4 by wraparound as the block data meets the burst length learned from the wraparound information WRPA. Thus, data outputted from the synchronous DRAM 2 does

not need to be sorted by the aligner, and the restriction where the top boundary of the data block that undergoes burst operations is fixed to the start access address does not need to be provided. Accordingly, even when using the memory burstable in a size shorter than the cache line length of the cache memory and having a wraparound function, the microprocessor 1 can shorten waiting time of the CPU until acquiring data in a cache miss, and therefore it can contribute to the enhanced data processing performance.

Additionally, the cache control part 5 can advance the cache fill operation as following the operation where the memory control part 6 sequentially reads data out of the synchronous DRAM 2 in burst operations in response to a cache mishit. Thus, the high-speed cache fill operation can be assured.

In view of the fact that a program or certain data is often located at sequential addresses, as described above, as for access except the first access among a plurality of access in burst operations, data to be accessed first by the CPU is allowed to arrive at the cache memory or CPU first in continuous data access when the memory is accessed from the top boundary defined by burst length. Therefore, it is useful to enhance the data processing performance.

The data processing system exemplified in Fig. 1 has one synchronous DRAM 2 connected to the microprocessor 1. When

a burst length (16 bytes, for example) relatively shorter than the cache line length (32 bytes, for example) of the cache memory 4 is set in the synchronous DRAM 2, a plurality of block data outputted by wraparound from the synchronous DRAM 2 performing the burst access operation can be joined and filled in the cache memory 4. Furthermore, in the case where write through is adopted as one process for the cache write hit of the cache memory 4, when write data is written into the synchronous DRAM 2 from the write thorough buffer shorter than the cache line length (eight bytes, for example), there are fewer unnecessary data transfer cycles because of the relatively shorter burst length. For eight bytes in the latter half of the burst access operation at this time, the data masking signal DM masks data, whereby the actual data write operation can be suppressed.

Accordingly, the data processing system does not impair the performance of efficiently transferring high capacity data of 32 bytes to the cache memory 4, it can suppress unnecessary cycles to the minimum in transferring relatively small data such as the data write through operation of the write through buffer, and thus it can enhance the data processing performance.

Fig. 10 depicts another example of the data processing device. The data processing system shown in the same drawing is provided with memories burstable by wraparound, such as two

synchronous DRAMs 2A and 2B. Both the synchronous DRAMs 2A and 2B have the same configuration as the synchronous DRAM 2. The synchronous DRAM 2A, one of them, is set up with a burst length of 16 bytes, whereas the synchronous DRAM 2B, the other of them, is set up with a burst length of 32 bytes. The CPU 3 independently sets the burst length of each of the synchronous DRAMs 2A and 2B in the mode registers of the synchronous DRAMs 2A and 2B by software after power on reset. At this time, the memory control registers 23 inside the memory control part 6 are set up with bus control information for a burst length of external memories such as the synchronous DRAMs 2A and 2B. The other configurations are the same as Fig. 1, omitting the detailed description.

According to the data processing system shown in Fig. 10, when a burst length (16 bytes, for example) relatively shorter than the cache line length (32 bytes, for example) of the cache memory 4 is set in the synchronous DRAM 2A, a plurality of block data outputted by wraparound from the synchronous DRAM 2A can be joined and filled in the cache memory 4. When the synchronous DRAM 2B set up with the burst length equal to the cache line length is included in the data processing system, the cache fill operation corresponding to the burst length of the synchronous DRAM 2B is also allowed in processing a cache mishit for the synchronous DRAM 2B.

Additionally, in the case where write through is adopted

as the process for a cache write hit of the cache memory 4, when write data is written into the synchronous DRAM 2A from the write through buffer shorter than the cache line length (eight bytes, for example), there are fewer unnecessary data transfer cycles because of the relatively shorter burst length. For 12 bytes in the latter half of the burst access operation at this time, the data masking signal DM can mask data to suppress the actual data write operation. When the synchronous DRAM 2B set up with the burst length equal to the cache line length is the object to be written by write through, unnecessary cycles are increased as compared with the synchronous DRAM 2A even when performing write mask. However, the amount of data to be accessed or transferred to the synchronous DRAM 2B at one time can be increased in a state that the synchronous DRAM 2B is temporarily removed from the object for cache, and thus the data processing system can contribute to the enhanced data processing performance. The control of temporarily removing the synchronous DRAM 2B from the object for cache can be performed by operation modes of the microprocessor 1 or by the CPU 3 to set the cache control register in the cache control part 5, not shown.

Accordingly, in the data processing system where a different burst length is set in a plurality of synchronous DRAMs, it can suppress unnecessary cycles as much as possible in transferring data of eight bytes, relatively small, without

deteriorating the performance of efficiently transferring high capacity data of 32 bytes, and it can realize various connection configurations or utilization forms of a plurality of memories having a different burst length.

Furthermore, in the configuration of programs operated in the microprocessor 1, the synchronous DRAM 2B is allowed to hold data having a size equal to or greater than a program cord and a cache line length, and the synchronous DRAM 2A is allowed to hold data having a size smaller than a cache line length, whereby the enhanced processing performance of the microprocessor 1 can be intended as well.

The invention made by the inventors has been described in detail in accordance with the embodiments, but the invention is not limited thereto. It is needless to say that the invention can be modified variously within the scope of the teachings, not deviating it.

For example, the cache memory may be for storing programs, or for storing data and programs as mixed. Additionally, for the cache memory, the associative memory format such as set associative, full associative or direct map can be adopted. Furthermore, for the cache memory, the write back method may be adopted instead of the write through method.

Moreover, the data processing device may be integrated with other computing units such as a floating point processing unit, other bus master modules such as a direct memory access

controller, or other peripheral circuits such as a timer or RAM. The burstable memory is not defined to the synchronous DRAM; it may be a synchronous SRAM. The number of burstable memories included in the data processing system may be increased properly.

The invention can be widely adapted to a data processing device capable of having access to a burstable memory and the data processing system. For example, it can be adapted to various data processing devices formed with a semiconductor integrated circuit such as a microprocessor, a microcomputer, a data processor, and a DSP.

What is claimed is:

1. A data processing device comprising:

a cache memory;

a cache control part for controlling the cache memory; and

a memory control part accessible to a memory in response to a cache mishit of the cache memory,

wherein in having access to a memory burstable in response to a cache mishit, the memory control part forms first information for indicating a burst length of the memory and it can control a single or plurality of burst operations necessary to obtain a data length meeting a cache line length according to the first information, and

the cache control part can control a cache fill operation of filling data acquired in the single or plurality of burst operations in the cache memory so as to locate the data in order of addresses according to the first information.

2. The data processing device according to claim 1, wherein in the cache fill operation, the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter of data acquired in burst operations by the memory control part, and the cache control part generates a cache fill

address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meant by the first information.

3. The data processing device according to claim 1, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the memory control part controls a burst operation starting from a top of a boundary of a data block defined by the burst length in subsequent burst operations.

4. A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a memory connected to the data processing device, the memory being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a cache line length of L bytes,

the memory is burstable in a range of a burst length in bytes, where L times one over two to the n-th power (n is a

natural number), and

the data processing device forms first information for indicating a burst length of the memory to a cache line length of the cache memory in response to a cache mishit of the cache memory, the data processing device allows the memory into burst operations for a single or plurality of times necessary to obtain a data length meeting the cache line length according to the first information, and the data processing device performs control of returning data of L bytes thereby obtained to the cache memory so as to arrange the data in order of addresses according to the first information.

5. A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a plurality of memories connected to the data processing device, the plurality of memories being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a cache line length of L bytes,

the plurality of memories is burstable in a range of a burst length in bytes, where L times one over two to the n-th power (n is a natural number), and the burst length is allowed to be set in each of the plurality of memories by the data processing device, and

the data processing device establishes a memory with data in a cache mishit as an object to be accessed in response to a cache mishit of the cache memory, and the data processing device performs control in which the data processing device forms first information for indicating a burst length of the memory to be accessed to a cache line length of the cache memory, the data processing device allows the memory into burst operations for a single or plurality of times necessary to obtain a data length meeting the cache line length according to the first information, and the data processing device returns data of L bytes thereby obtained so as to locate the data in order of addresses according to the first information.

6. The data processing system according to claim 4 or 5, wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

7. The data processing system according to claim 4 or 5, wherein in cache fill operation, the data processing device generates a synchronization signal synchronous with a delimiter of data acquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in

synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meant by the first information.

8. The data processing system according to claim 4 or 5, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent bust operations.

9. A data processing system comprising:

a CPU;

a cache memory accessible by the CPU;

a cache control part for controlling the cache memory;

a memory control part accessible to a memory in response to a cache mishit of the cache memory; and

a memory connected to the memory control part, the memory being burstable,

wherein in having access to the memory in response to a cache mishit, the memory control part generates first information for indicating a burst length of the memory to a

cache line length of the cache memory, and the memory control part can control a single or plurality of burst operations necessary to obtain a data length meeting the cache line length according to the first information, and

the cache control part can control a cache fill operation of filling data acquired in the single or plurality of burst operations in the cache memory so as to locate the data in order of addresses by wraparound according to the first information.

10. The data processing system according to claim 9, wherein in the cache fill operation the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter of data acquired in the burst operation by the memory control part, the cache control part controls wraparound starting from the address information in a range of a burst length meant by the first information, and the cache control part generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal.

11. The data processing system according to claim 10, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a burst operation by wraparound starting from a data location at an address in the cache mishit in a first burst operation,

and the memory control part controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

ABSTRACT OF THE DISCLOSURE

A data processing device has a CPU, a cache memory, a cache control part, and a memory control part accessible to a memory in response to a cache mishit of the cache memory. In having access to a burstable memory in response to a cache mishit, a memory control part generates first information for indicating a burst length of the memory to a cache line length of the cache memory, and it can control a single or plurality of burst operations necessary to obtain a data length meeting the cache line length according to the first information. The cache control part can control the operation of filling data acquired in the single or plurality of burst operations in the cache memory by wraparound according to the first information. Data outputted from the memory does not need to be sorted by an aligner and there is no need to provide the restriction of fixing the top boundary of a data block for burst operations to a start access address. Therefore, waiting time of the CPU until acquiring data in a cache miss can be shortened even when using a memory with a burst length shorter than the cache line length.

FIG.1

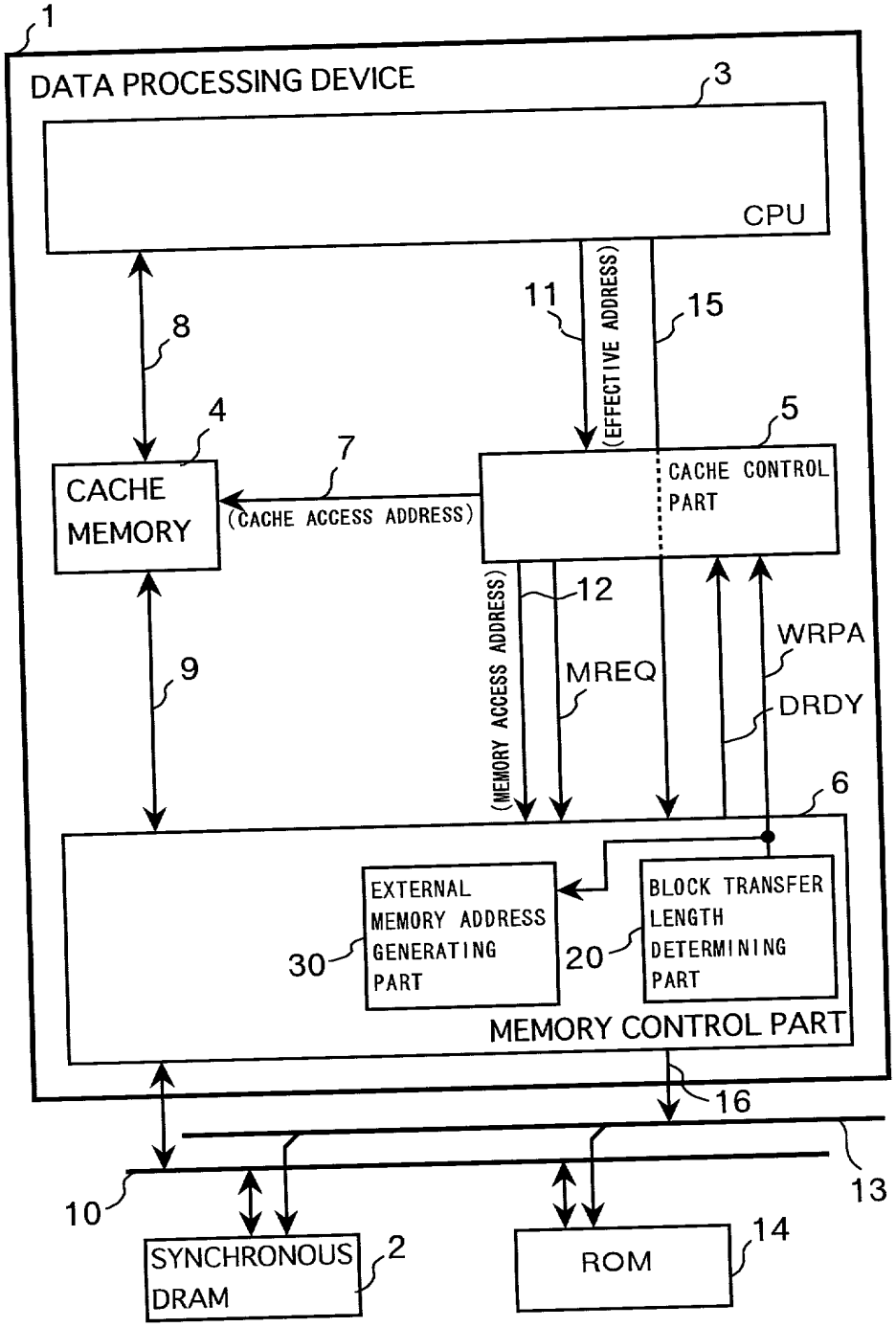
1
DATA PROCESSING DEVICE
3
CPU
8
11
(EFFECTIVE ADDRESS)
15
4
5
CACHE MEMORY
7
(CACHE ACCESS ADDRESS)
CACHE CONTROL PART
12
WRPA
9
MREQ
DRDY
(MEMORY ACCESS ADDRESS)
6
EXTERNAL MEMORY ADDRESS GENERATING PART
30
20
BLOCK TRANSFER LENGTH DETERMINING PART
MEMORY CONTROL PART
16
13
10
SYNCHRONOUS DRAM
2
ROM
14

FIG.2

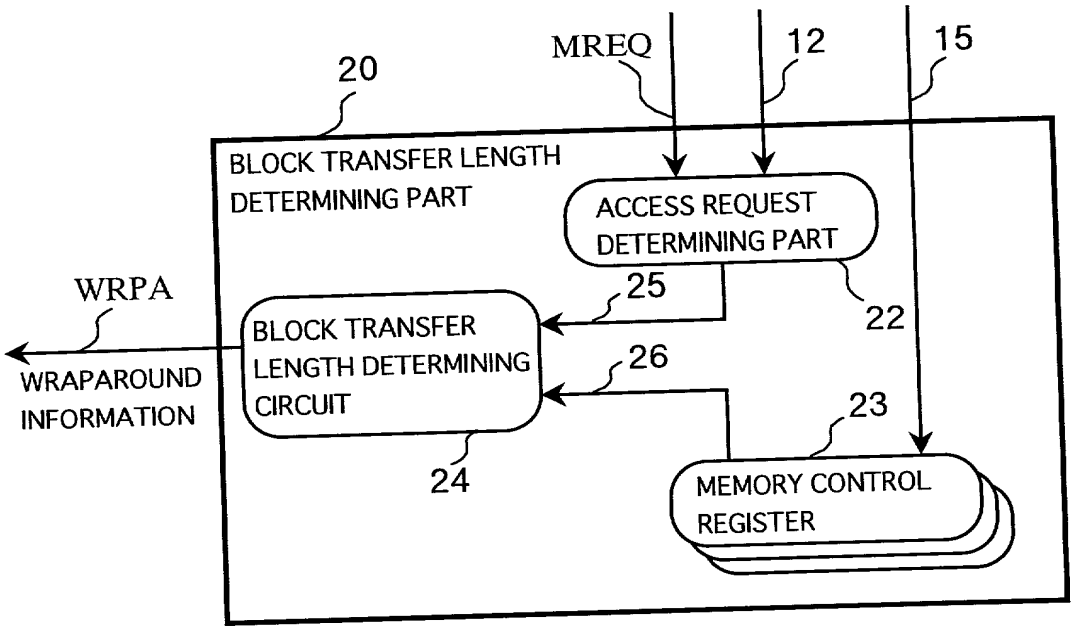
MREQ
12
15
20
BLOCK TRANSFER LENGTH DETERMINING PART
ACCESS REQUEST DETERMINING PART
25
22
WRPA
BLOCK TRANSFER LENGTH DETERMINING CIRCUIT
26
WRAPAROUND INFORMATION
23
24
MEMORY CONTROL REGISTER

FIG.3

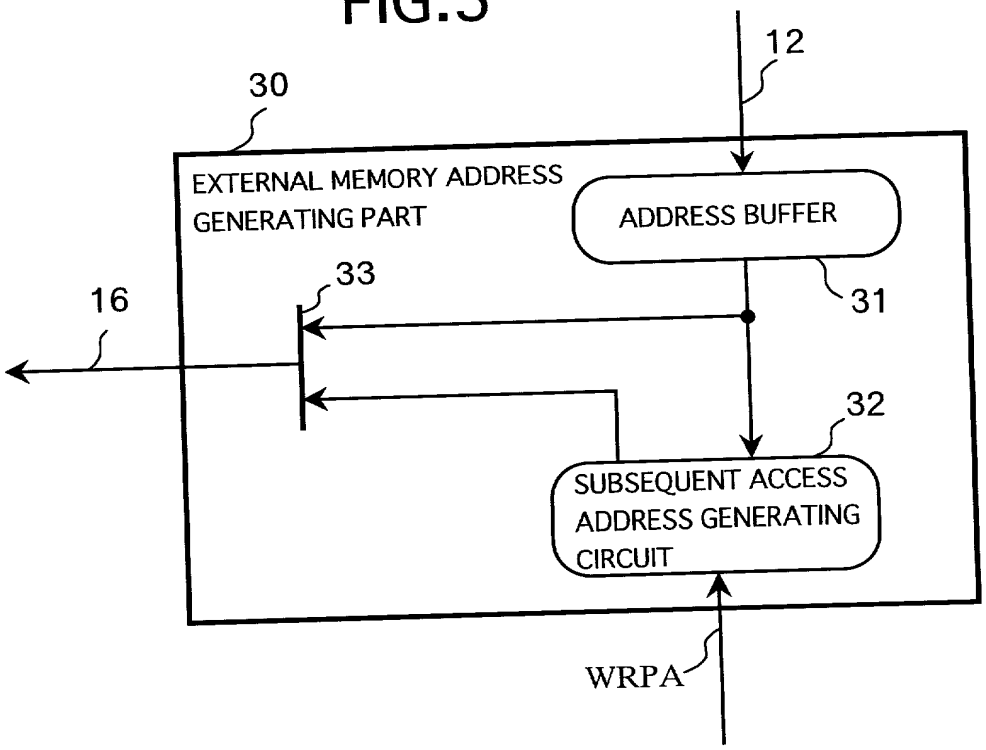
12
30
EXTERNAL MEMORY ADDRESS GENERATING PART
ADDRESS BUFFER
33
16
31
32
SUBSEQUENT ACCESS ADDRESS GENERATING CIRCUIT
WRPA

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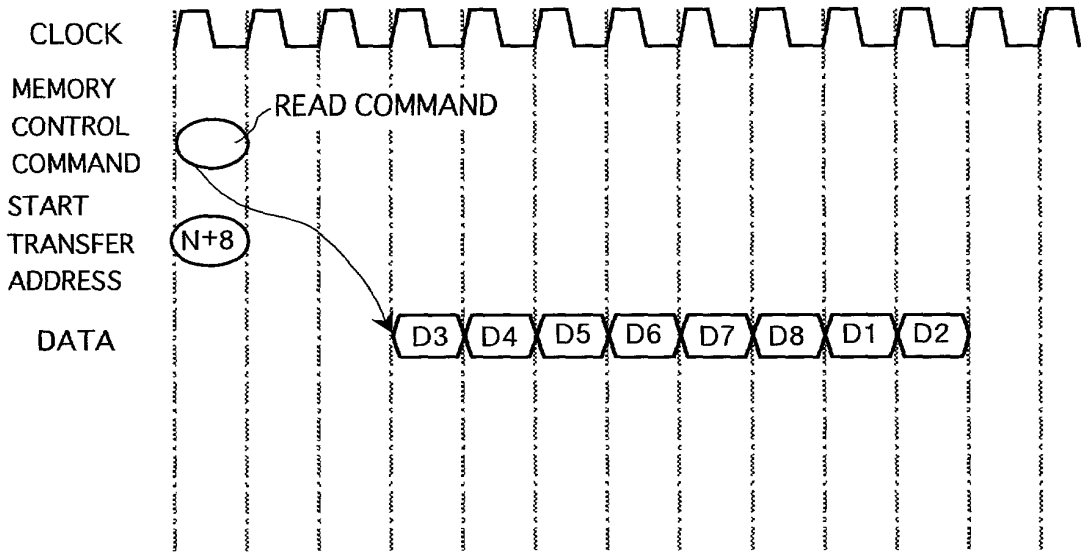
FIG.4

	N	N+4	N+8	N+12	N+16	N+20	N+24	N+28
ADDRESS N	D1	D2	D3	D4	D5	D6	D7	D8

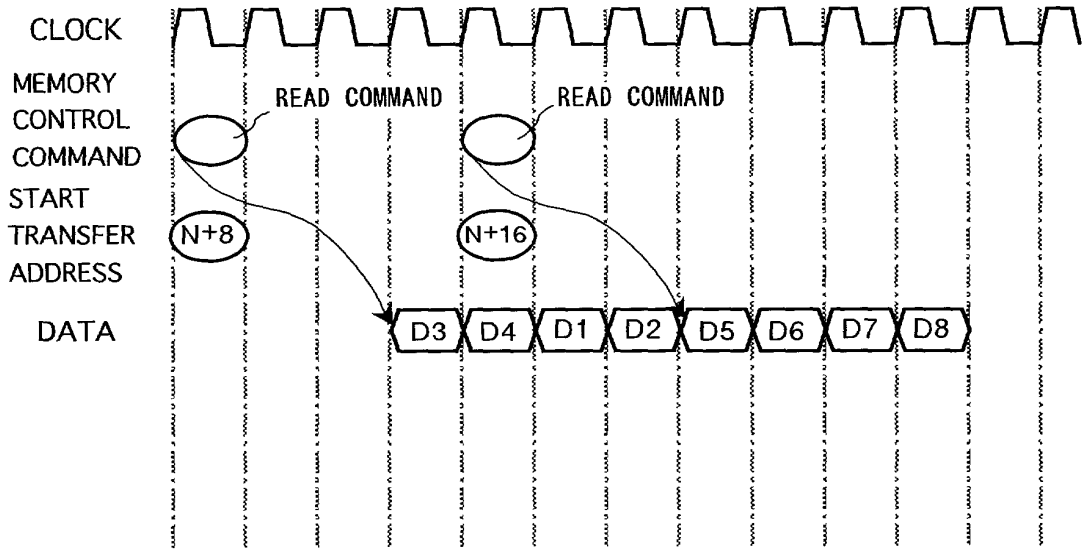
FIRST ACCESS ADDRESS	WRAPAROUND INFORMATION	SECOND ACCESS ADDRESS
N+0	32 BYTES	NO
	16 BYTES	N+16
N+4 N+8 N+12	32 BYTES	NO
	16 BYTES	N+16
N+16	32 BYTES	NO
	16 BYTES	N+0
N+20 N+24 N+28	32 BYTES	NO
	16 BYTES	N+0

FIG.5



(BURST TRANSFER FROM ADDRESS OF N+8, WRAPAROUND LENGTH=32BYTES)

FIG.6



(BURST TRANSFER FROM ADDRESS OF N+8, WRAPAROUND LENGTH=16BYTES)

FIG.7

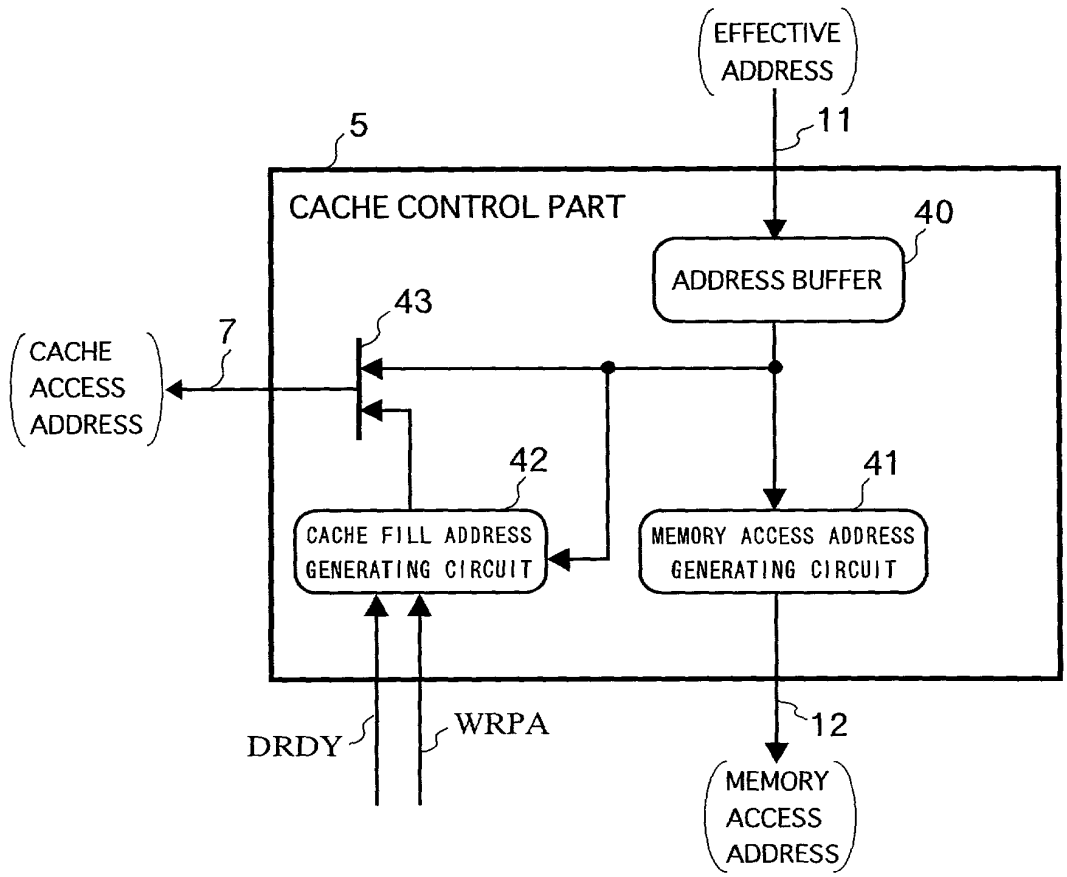

EFFECTIVE ADDRESS
11
5
CACHE CONTROL PART
40
ADDRESS BUFFER
43
7
CACHE ACCESS ADDRESS
42
41
CACHE FILL ADDRESS GENERATING CIRCUIT
MEMORY ACCESS ADDRESS GENERATING CIRCUIT
DRDY
WRPA
12
MEMORY ACCESS ADDRESS

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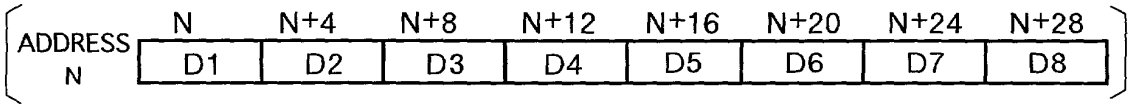
FIG.8



EFFECTIVE ADDRESS	WRAPAROUND INFORMATION	CACHE FILL ADDRESS (UPPER) CORRESPONDING DATA (LOWER)
N+0	32 BYTES	N+0->N+4->N+8->N+12->N+16->N+20->N+24->N+28 D1 ->D2 ->D3 ->D4 ->D5 ->D6 ->D7 ->D8
	16 BYTES	N+0->N+4->N+8->N+12->N+16->N+20->N+24->N+28 D1 ->D2 ->D3 ->D4 ->D5 ->D6 ->D7 ->D8
N+8	32 BYTES	N+8->N+12->N+16->N+20->N+24->N+28->N+0->N+4 D3 ->D4 ->D5 ->D6 ->D7 ->D8 ->D1 ->D2
	16 BYTES	N+8->N+12->N+0->N+4->N+16->N+20->N+24->N+28 D3 ->D4 ->D1 ->D2 ->D5 ->D6 ->D7 ->D8
N+16	32 BYTES	N+16->N+20->N+24->N+28->N+0->N+4->N+8->N+12 D5 ->D6 ->D7 ->D8 ->D1 ->D2 ->D3 ->D4
	16 BYTES	N+16->N+20->N+24->N+28->N+0->N+4->N+8->N+12 D5 ->D6 ->D7 ->D8 ->D1 ->D2 ->D3 ->D4
N+24	32 BYTES	N+24->N+28->N+0->N+4->N+8->N+12->N+16->N+20 D7 ->D8 ->D1 ->D2 ->D3 ->D4 ->D5 ->D6
	16 BYTES	N+24->N+28->N+16->N+20->N+0->N+4->N+8->N+12 D7 ->D8 ->D5 ->D6 ->D1 ->D2 ->D3 ->D4

FIG.9

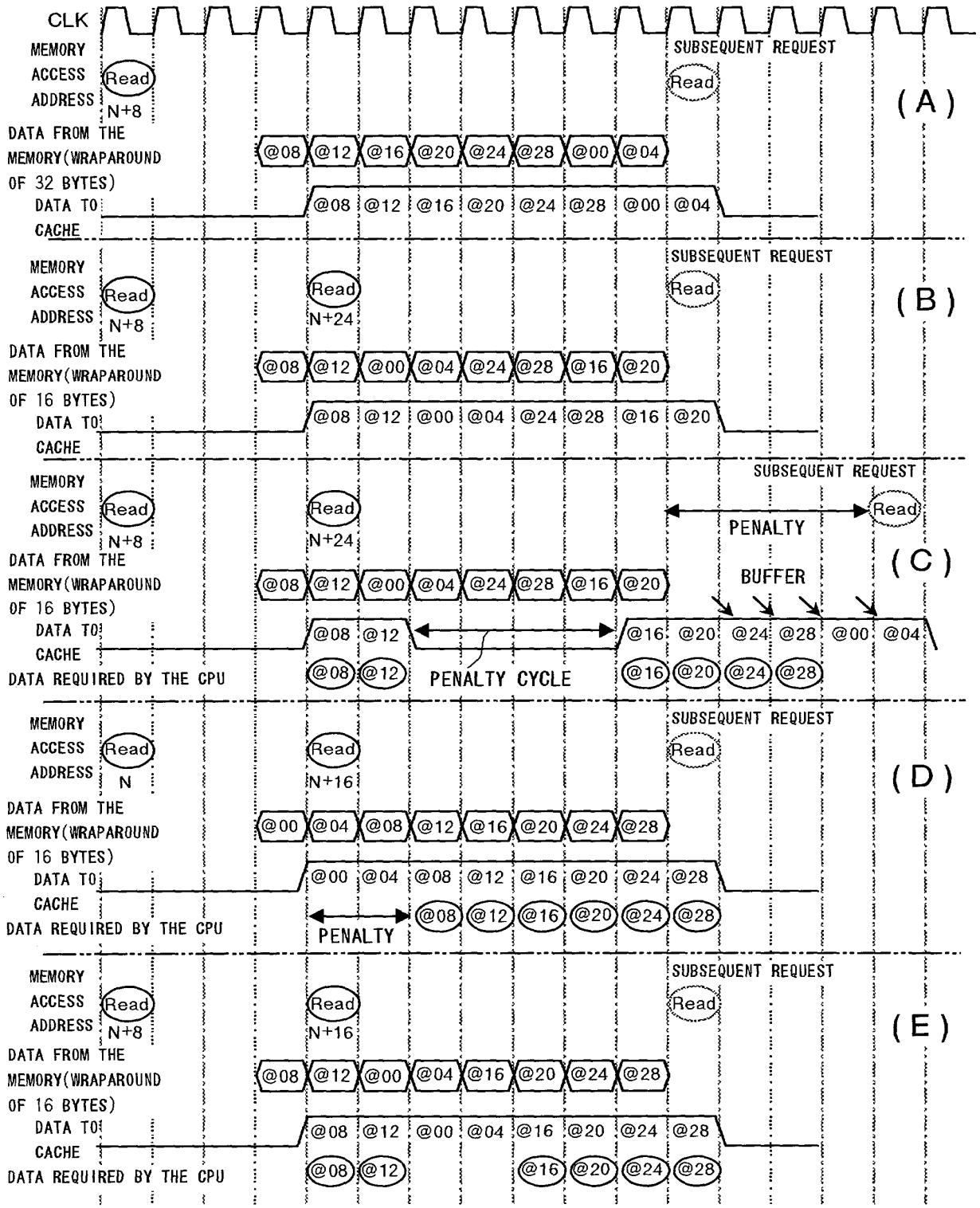

CLK
MEMORY ACCESS ADDRESS
Read
N+8
DATA FROM THE MEMORY(WRAPAROUND OF 32 BYTES)
@08 @12 @16 @20 @24 @28 @00 @04
DATA TO CACHE
SUBSEQUENT REQUEST
Read
(A)
N+24
@08 @12 @00 @04 @24 @28 @16 @20
OF 16 BYTES)
(B)
PENALTY
BUFFER
(C)
DATA REQUIRED BY THE CPU
PENALTY CYCLE
N
N+16
(D)
(E)

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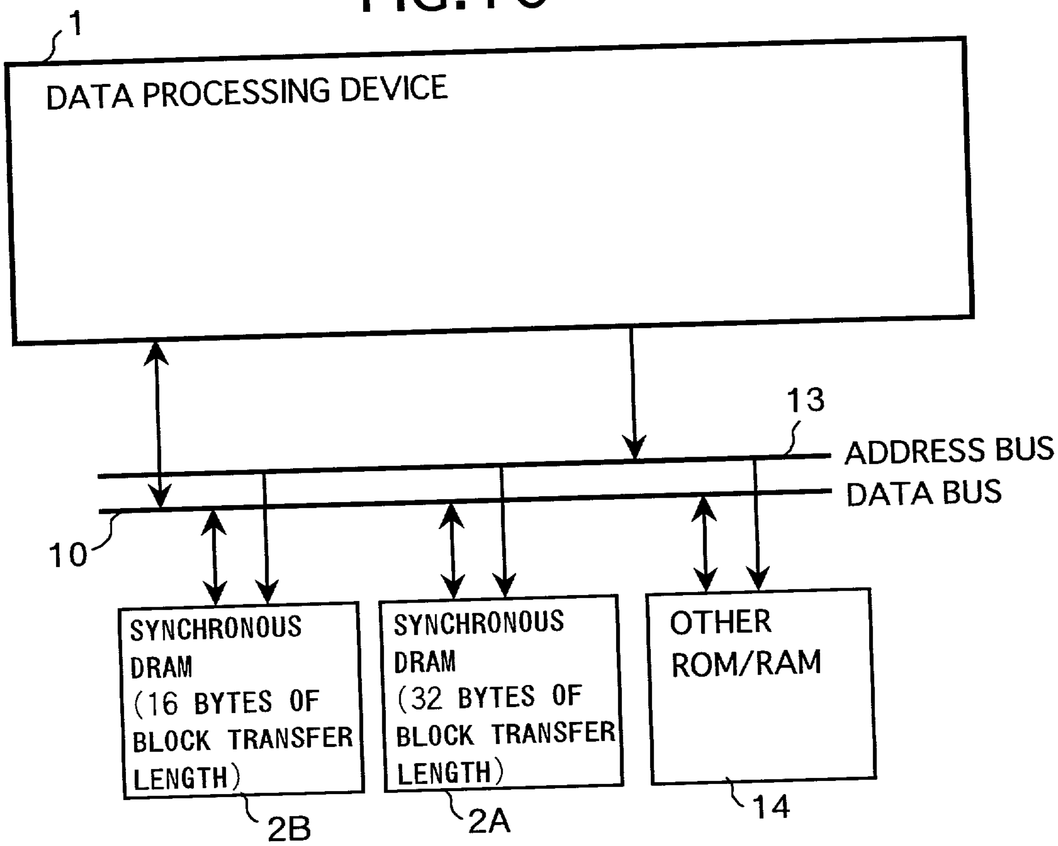
FIG.10



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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on 16 / November / 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/06371 and was amended on
28 / April / 2000 (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、 米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

2

Stanley P. Fisher, Reg. No. 24,344 and Juan Carlos Marquez, Reg. No. 34,072

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Telephone: (703)641-4211
Fax: (703)641-4340

唯一または第一発明者名 1-02	**Full name of sole or first inventor** Masayuki ITO
発明者の署名 日付	**Inventor's signature** Masayuki Ito **Date** 2/18/2002
住所	**Residence** Kodaira, Japan JP
国籍	**Citizenship** Japan
私書箱	**Post Office Address** c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

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第二共同発明者名 2-00	**Full name of second joint inventor, if any** Yutaka YOSHIDA
第二共同発明者の署名 日付	**Second inventor's signature** Yutaka Yoshida **Date** 2/18/2002
住所	**Residence** Kodaira, Japan JP
国籍	**Citizenship** Japan
私書箱	**Post Office Address** c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第三共同発明者名	**Full name of third joint inventor, if any**
第三共同発明者の署名 日付	**Third inventor's signature** **Date**
住所	**Residence**
国籍	**Citizenship**
私書箱	**Post Office Address**
第四共同発明者名	**Full name of fourth joint inventor, if any**
第四共同発明者の署名 日付	**Fourth inventor's signature** **Date**
住所	**Residence**
国籍	**Citizenship**
私書箱	**Post Office Address**
第五共同発明者名	**Full name of fifth joint inventor, if any**
第五共同発明者の署名 日付	**Fifth inventor's signature** **Date**
住所	**Residence**
国籍	**Citizenship**
私書箱	**Post Office Address**